wherein said wires are signal wires excluding power supply wires, and

said wire dummies are further provided in areas overlapping positions of said power supply wires that are provided in the first layer.

Q1

5. (AMENDED) A semiconductor integrated circuit, comprising:

a plurality of layers provided on a semiconductor substrate;

wires provided in a first layer that is one of said plurality of layers; and

wire dummies provided in a second layer different from the first layer and having an arrangement that avoids areas overlapping positions of said wires,

wherein said wires are signal wires excluding power supply wires,

said wire dummies are further provided in areas overlapping positions of said power supply wires that are provided in the first layer, and

said signal wires have a width less than a predetermined wire width, and said power supply wires have a width greater than the predetermined wire width.

Q2

8. (AMENDED) A semiconductor integrated circuit, comprising:

a wire layer;

wires provided in said wire layer; and

dummy patterns provided in said wire layer and having different sizes,

wherein said dummy patterns having different sizes are arranged at respective different pattern intervals.